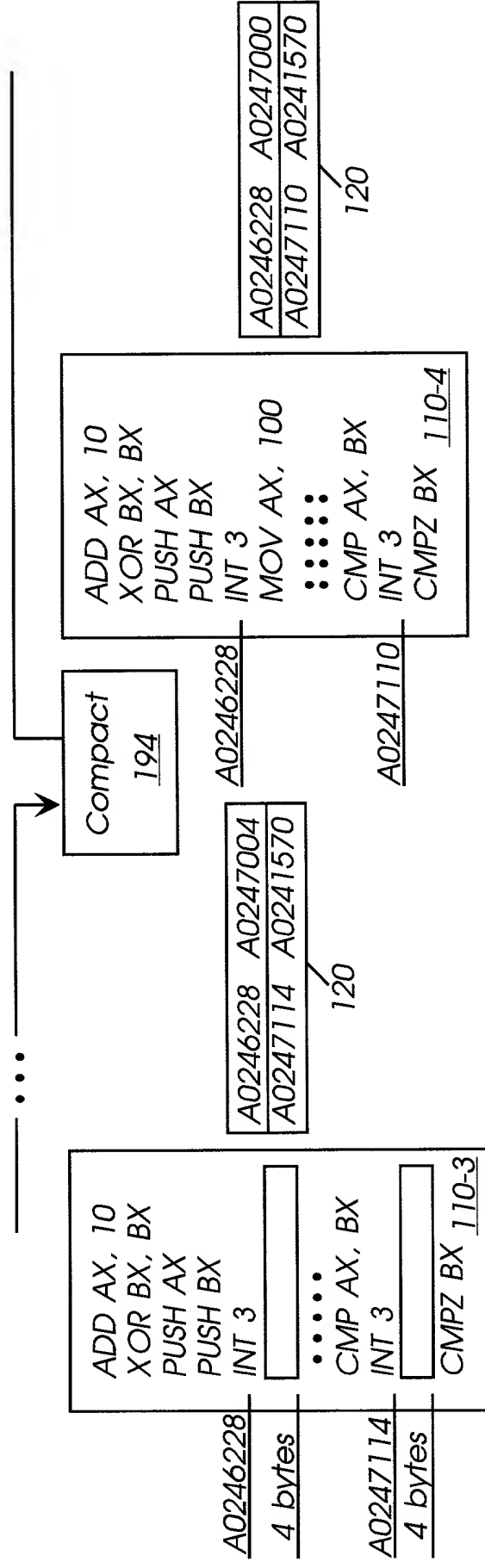


FIG. 1A



**FIG. 7B**

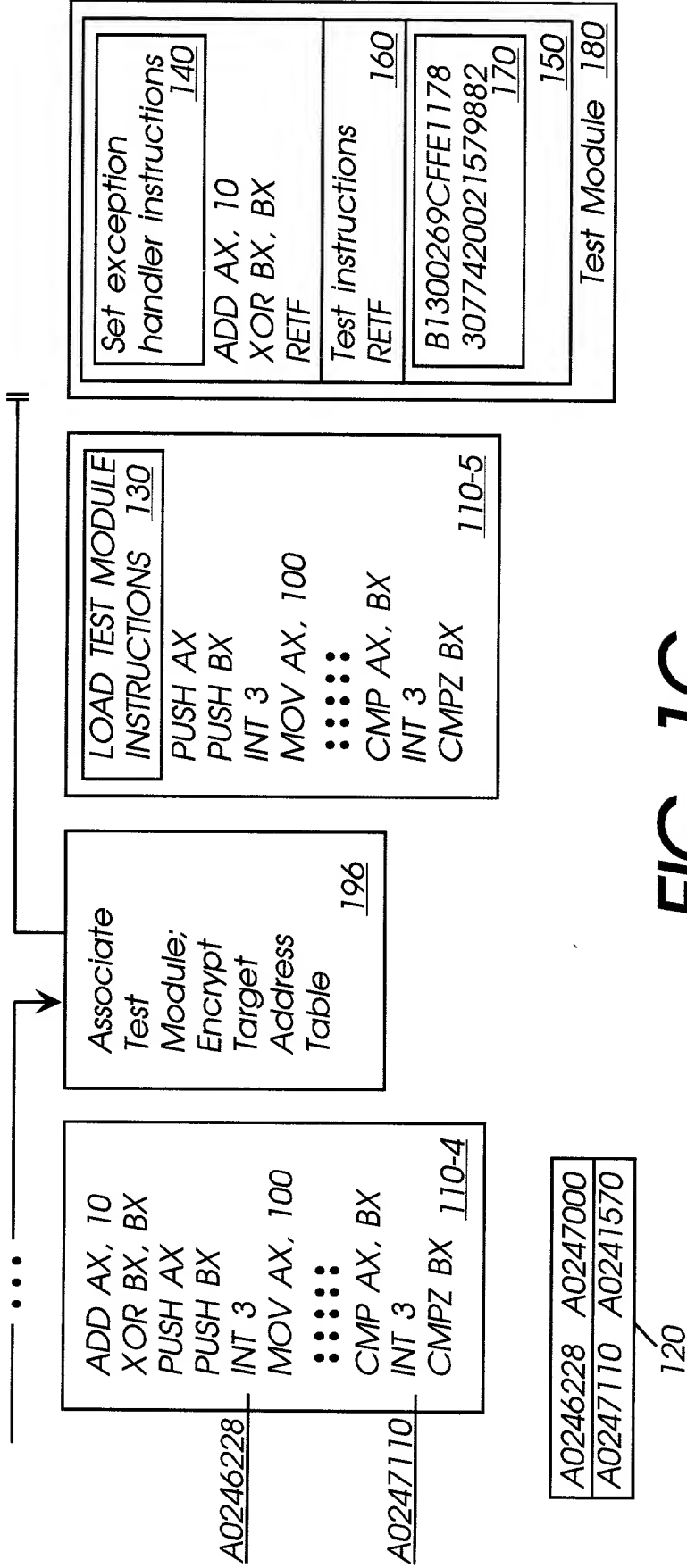


FIG. 1C

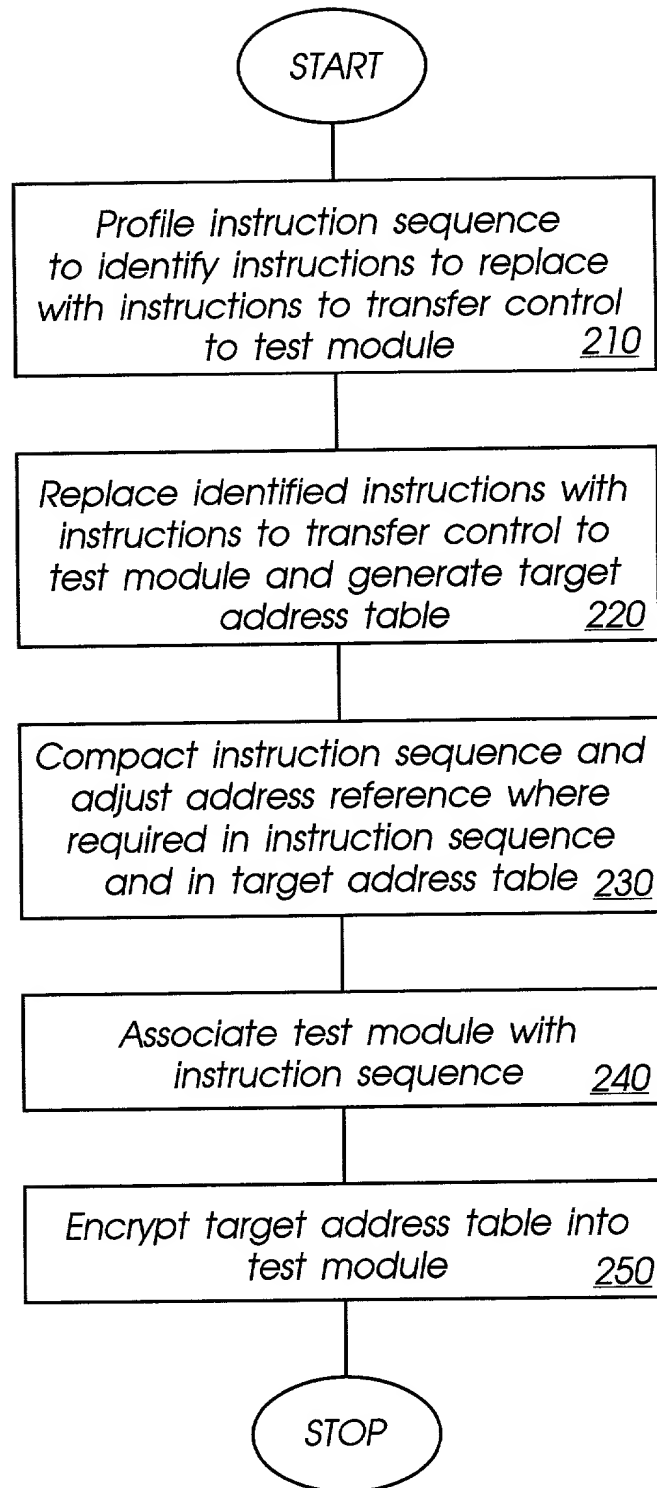


FIG. 2

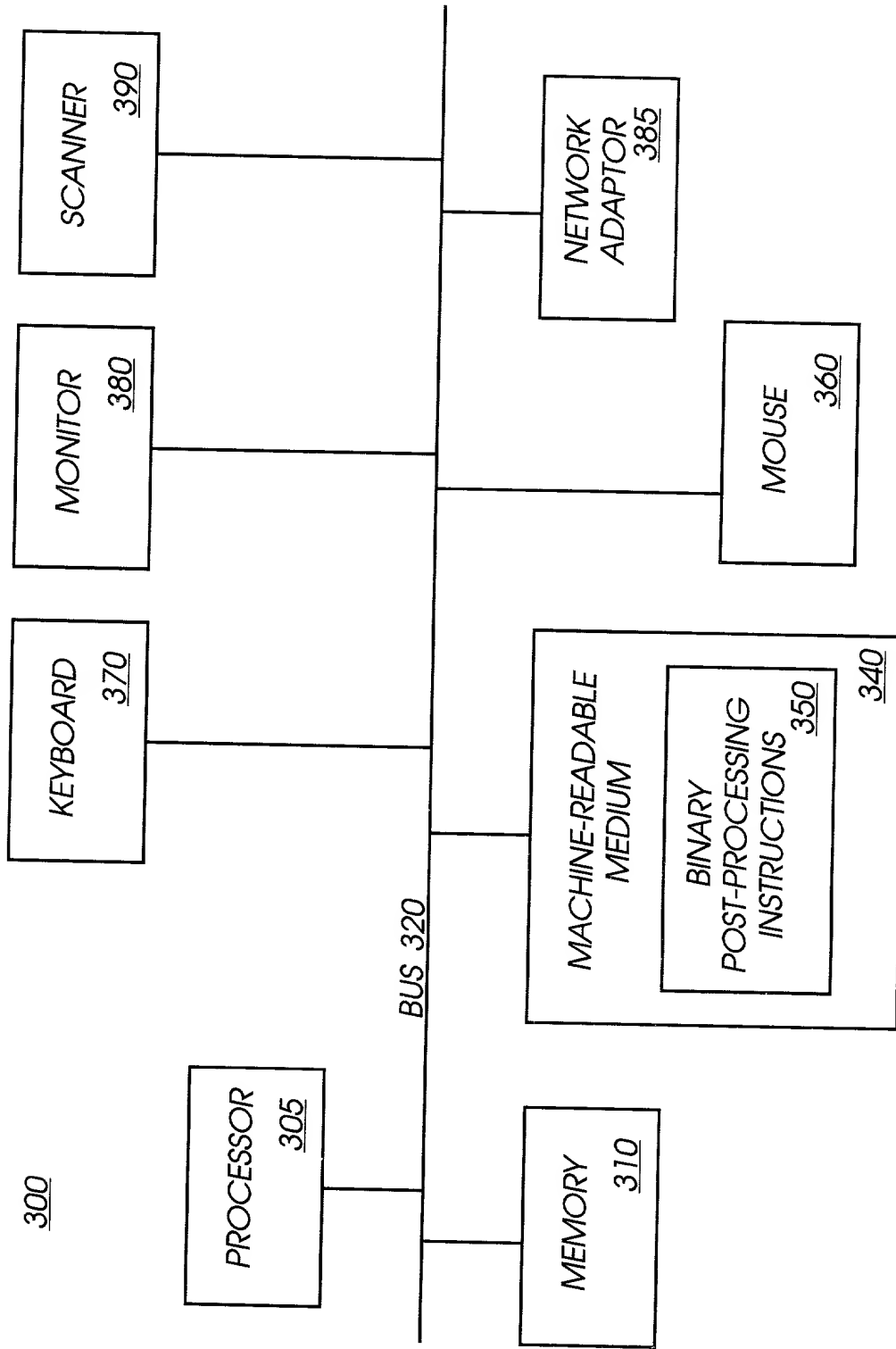


FIG. 3

*Machine-Readable  
Storage Medium*

*Binary Post-Processing  
Instructions*

*Instruction to identify instruction in  
instruction sequence to replace* 420

*Instructions to replace identified  
instructions with instructions to transfer control  
to test module* 430

*Instructions to generate target address table* 440

*Instructions to compact instruction sequence  
and adjust address reference in instruction  
sequence and target address table* 450

*Instructions to associate test module with  
instruction sequence* 460

*Instructions to encrypt target address  
table into test module* 470

410

400

**FIG. 4**

FIG. 5

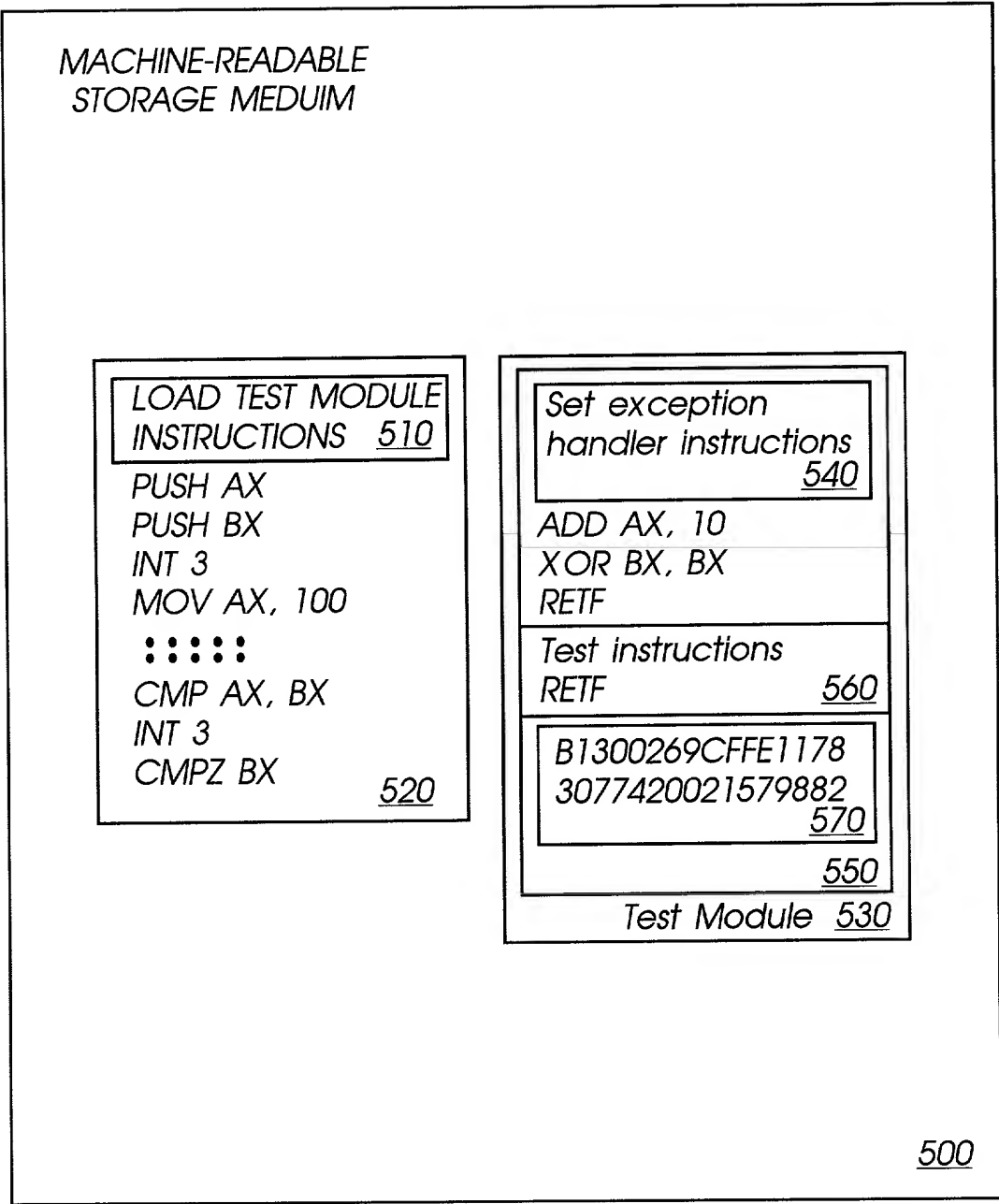


FIG. 5